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S/N 09/812,226

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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|-------------|--|-----------------|----------------|
| Applicant: | Sit, et al. | Examiner: | Unassigned |
| Serial No.: | 09/812,226 | Group Art Unit: | Unassigned |
| Filed: | March 19, 2001 | Docket No.: | 02316.1410US01 |
| Title: | Telecommunications Chassis, Module and Bridging Repeater Circuitry | | |

CERTIFICATE UNDER 37 CFR 1.8:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231 on October 29, 2001.


Jeramie J. Keys

SUBMISSION OF SUBSTITUTE DRAWINGS

Commissioner for Patents
Attn: Official Draftsman
Washington, D.C. 20231

Dear Sir:

In response to the Notice to File Corrected Application Papers, Applicant submits substitute drawings with the approximate margins in accordance with 37 CFR 1.84(g).

A copy of the Notice to File Corrected Application Papers is also enclosed.

Applicant believes that the submission of these papers completes the filing of all necessary papers and it is therefore respectfully requested that the enclosed documents be recorded in the U.S. Patent and Trademark Office.

Respectfully submitted,
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Minneapolis, Minnesota 55402-0903
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2004-04-09 10:00:00

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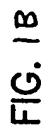


FIG. 2B

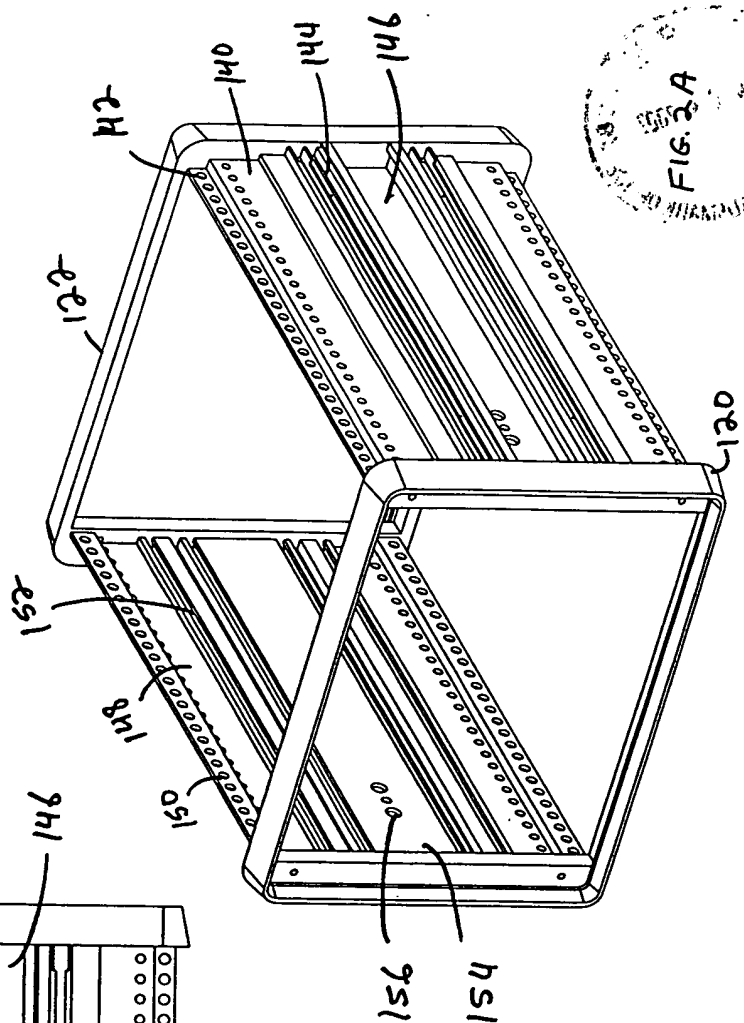
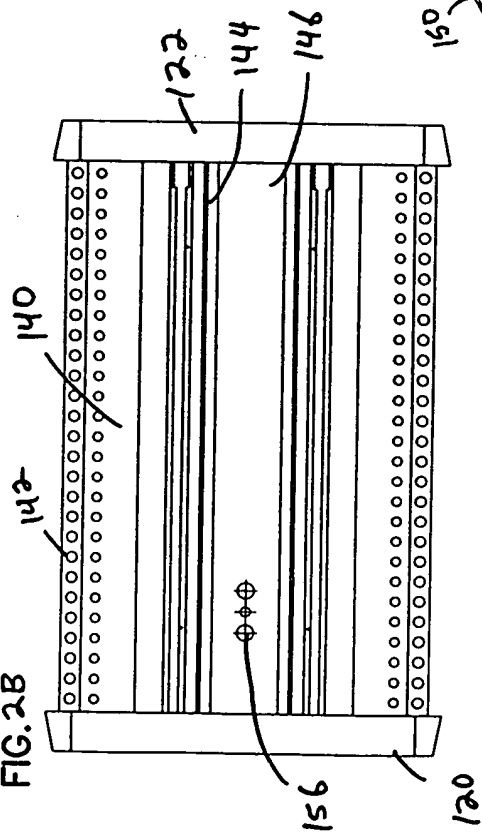


FIG. 2A



1. **Introduction**

2. **Background**

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253. **Supplementary Materials**

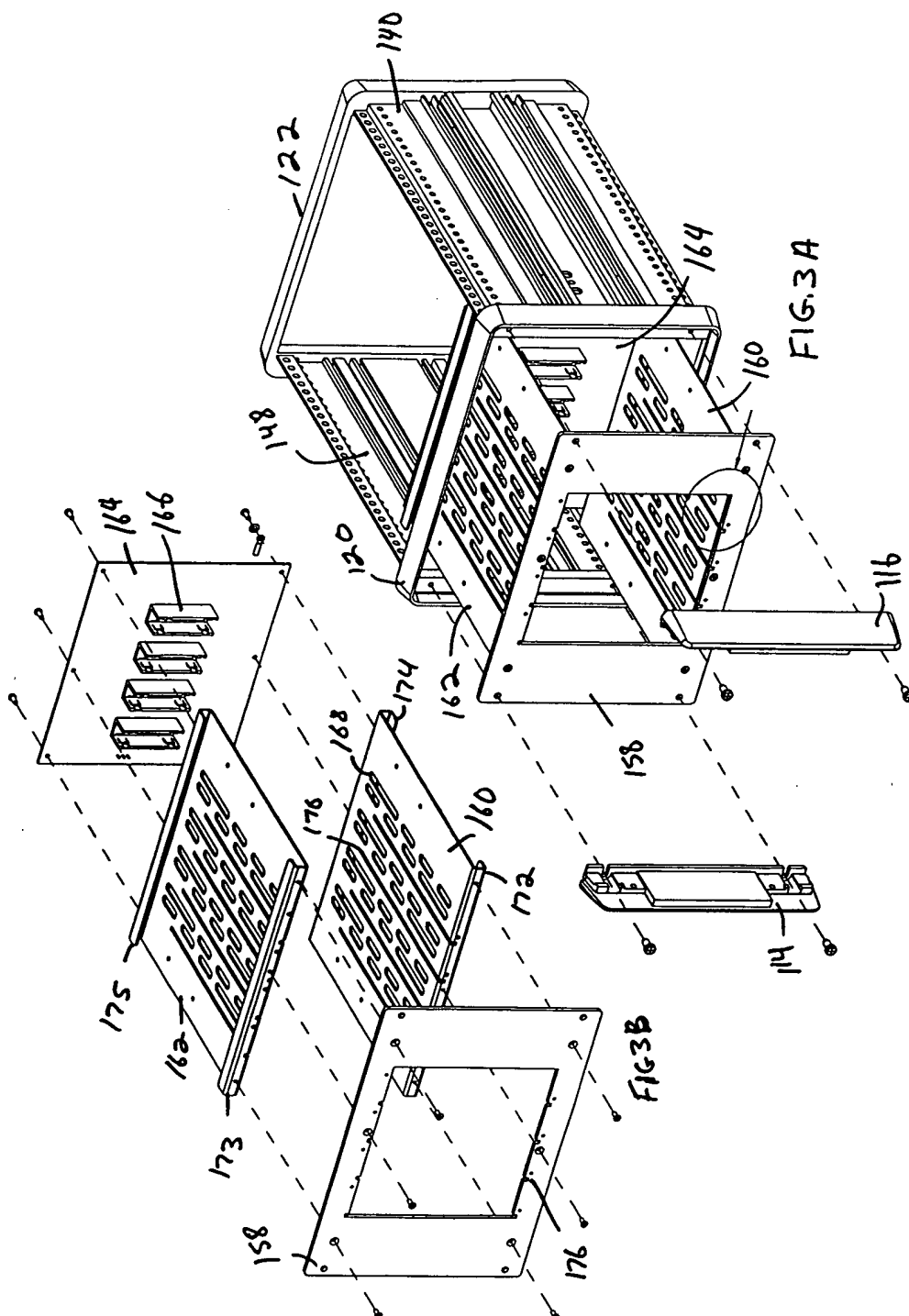
254. **Abbreviations**

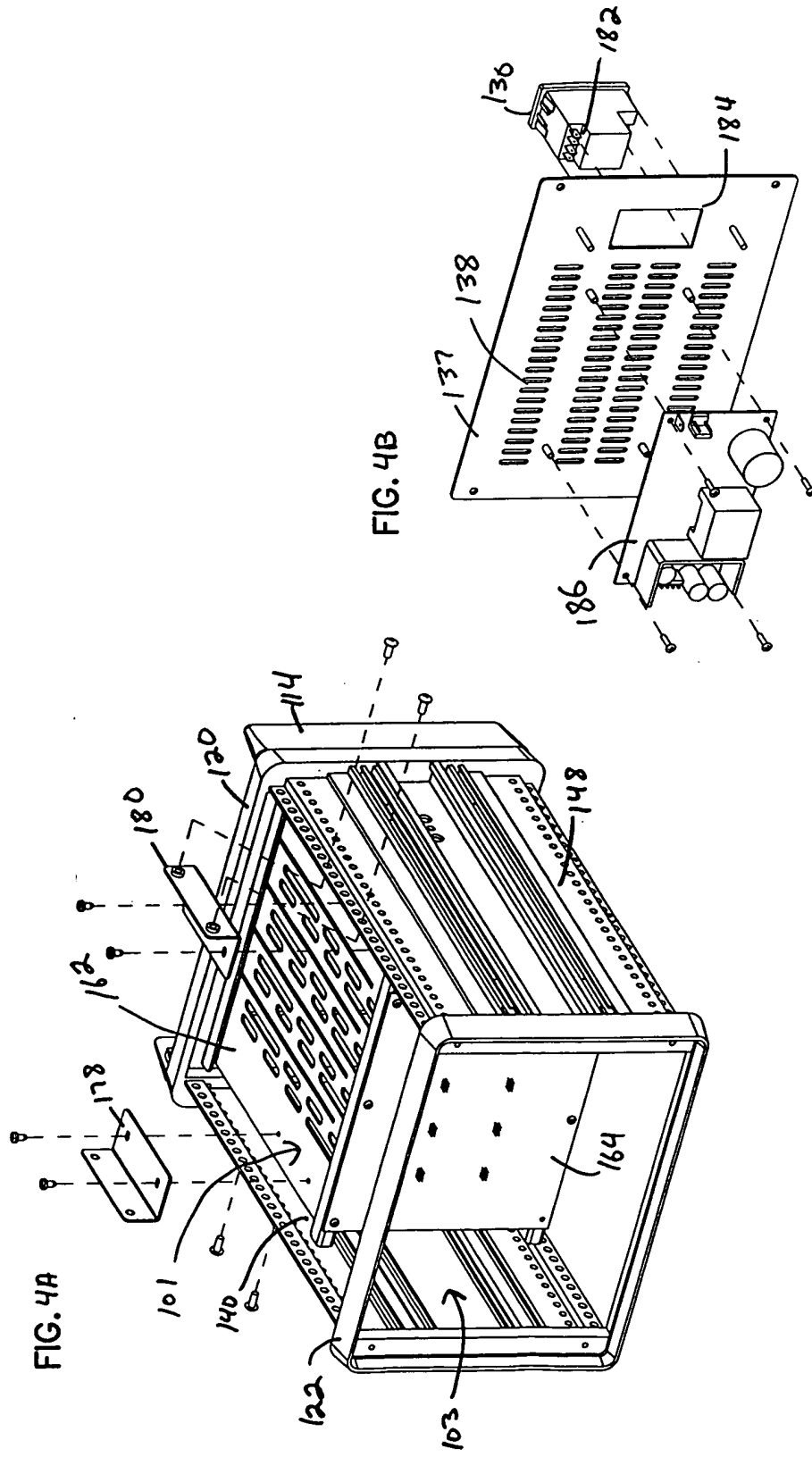
255. **Conflicts of Interest**

256. **Acknowledgments**

257. **Author Contributions**

258. **References**</





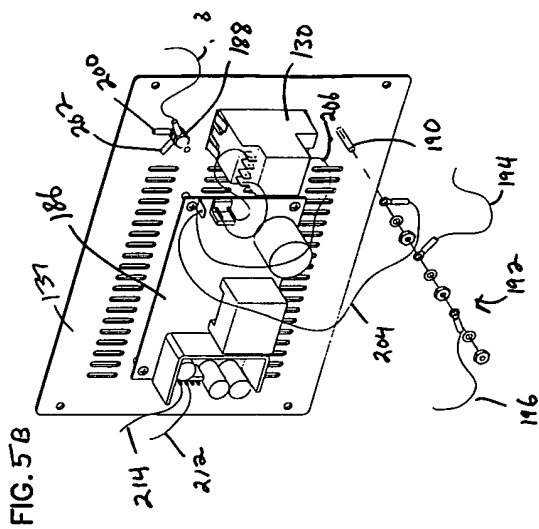
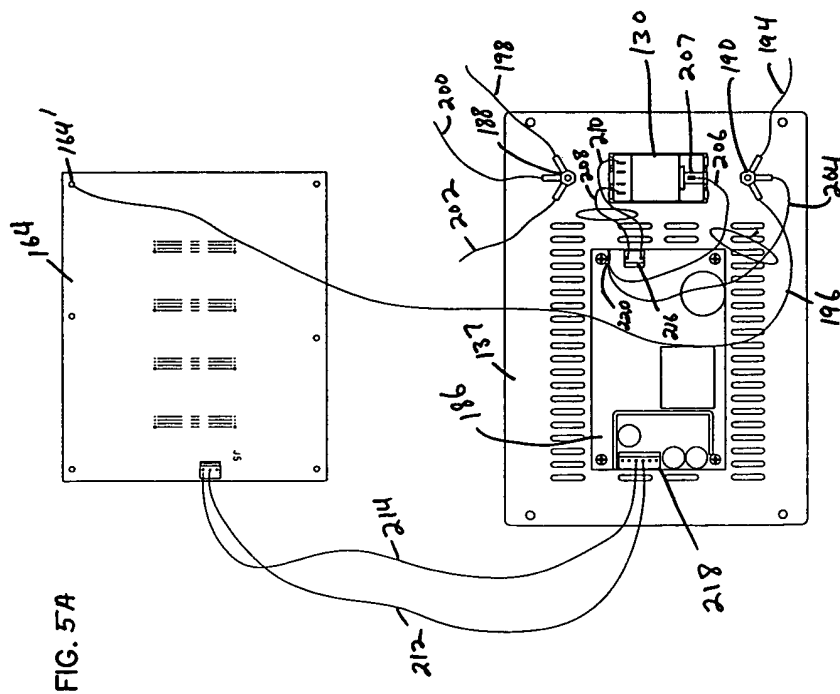
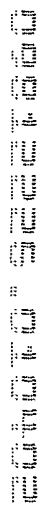
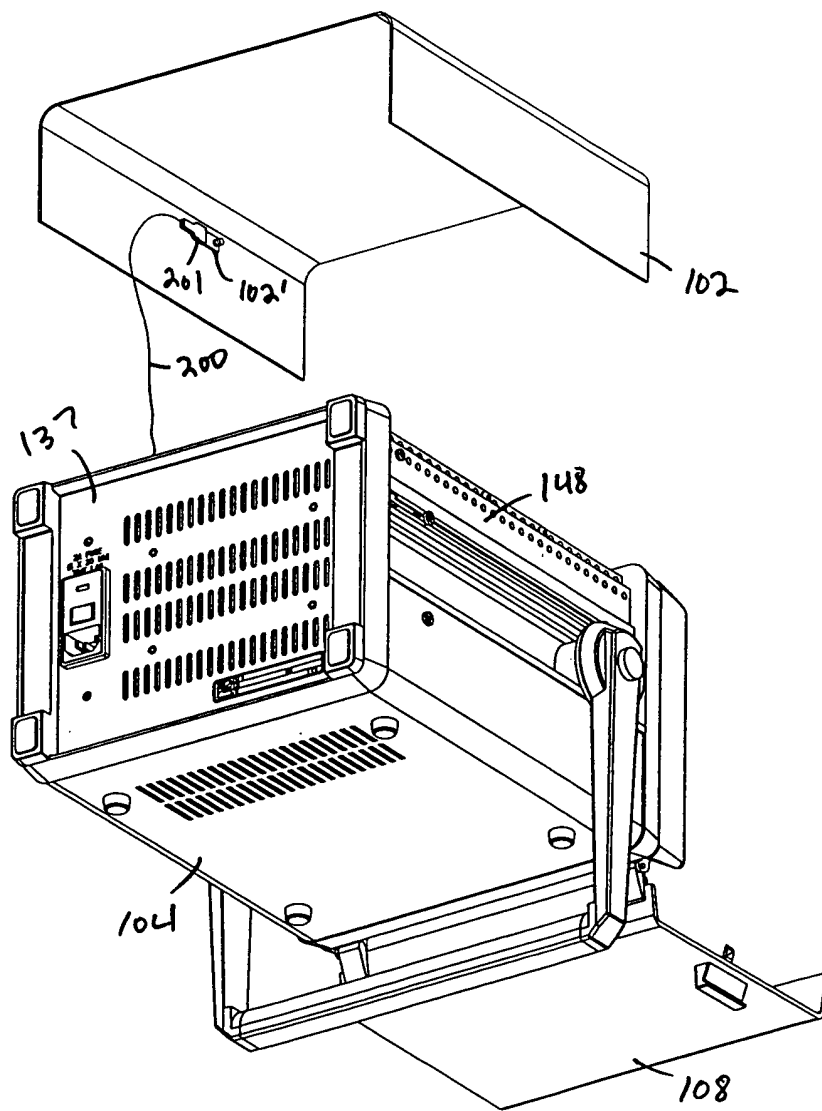




FIG. 5C



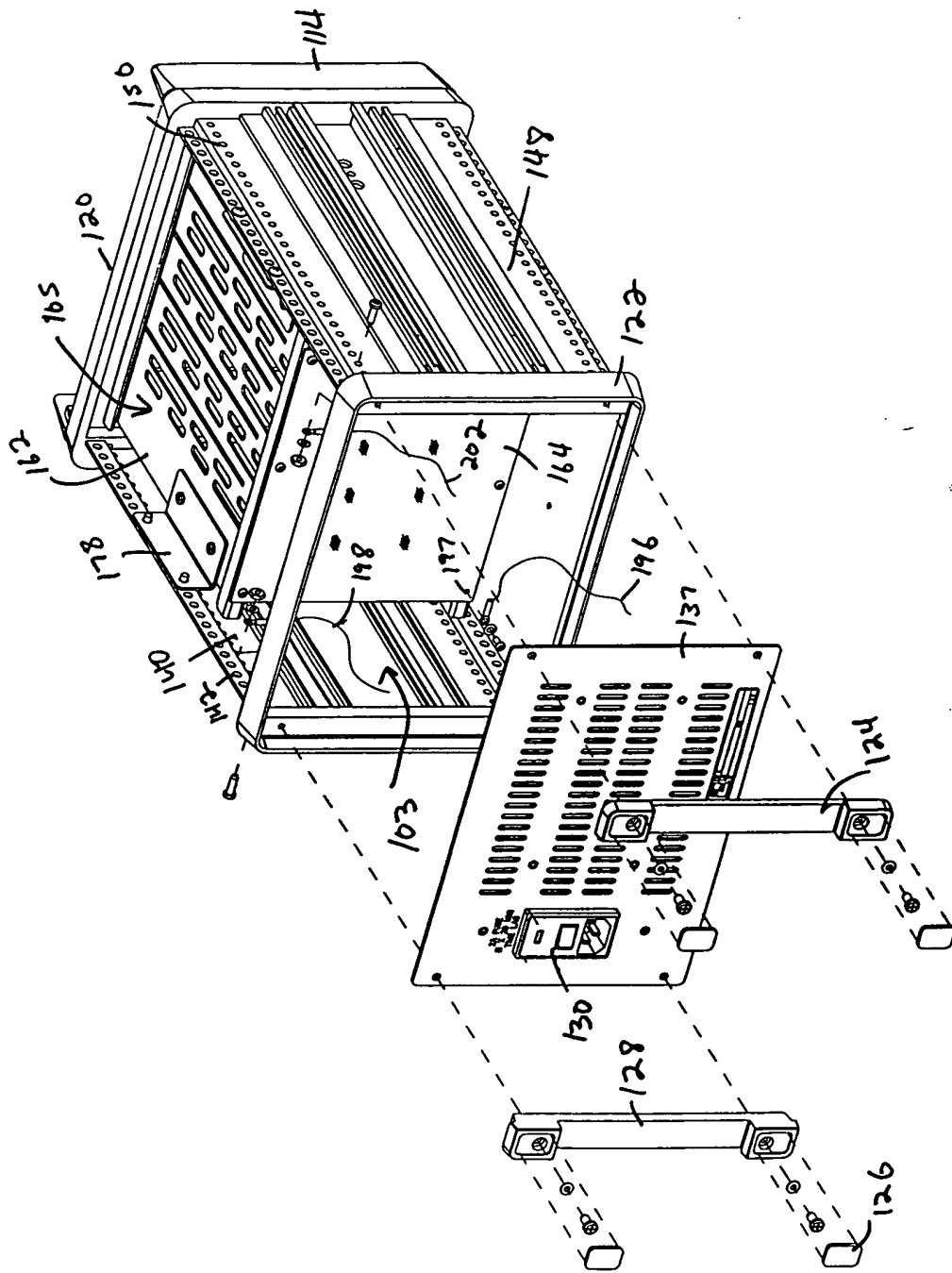


FIG. 6

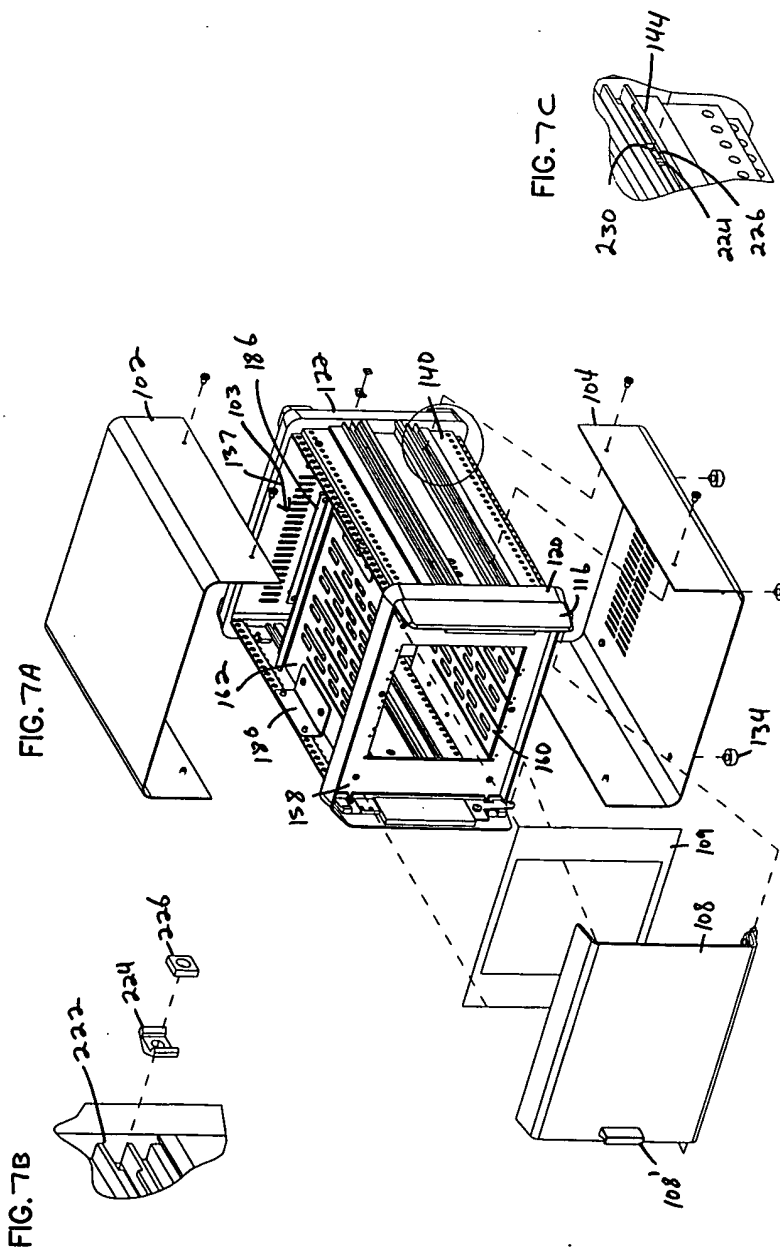


FIG. 8A

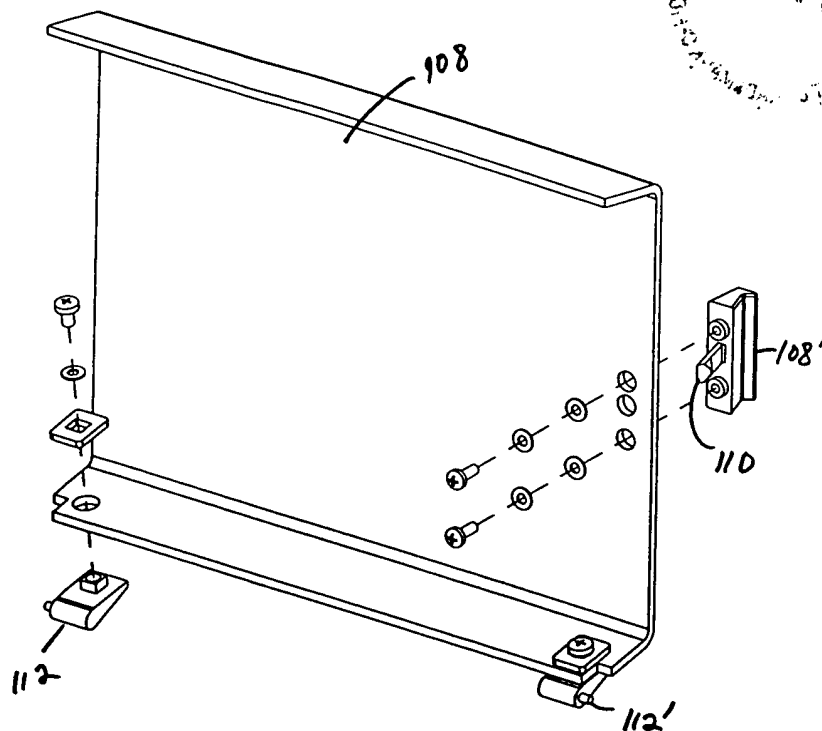
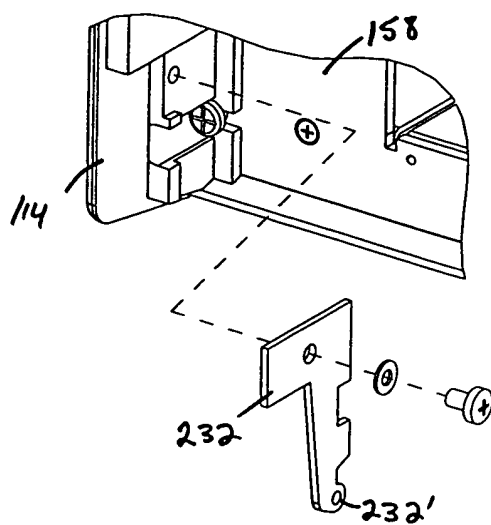
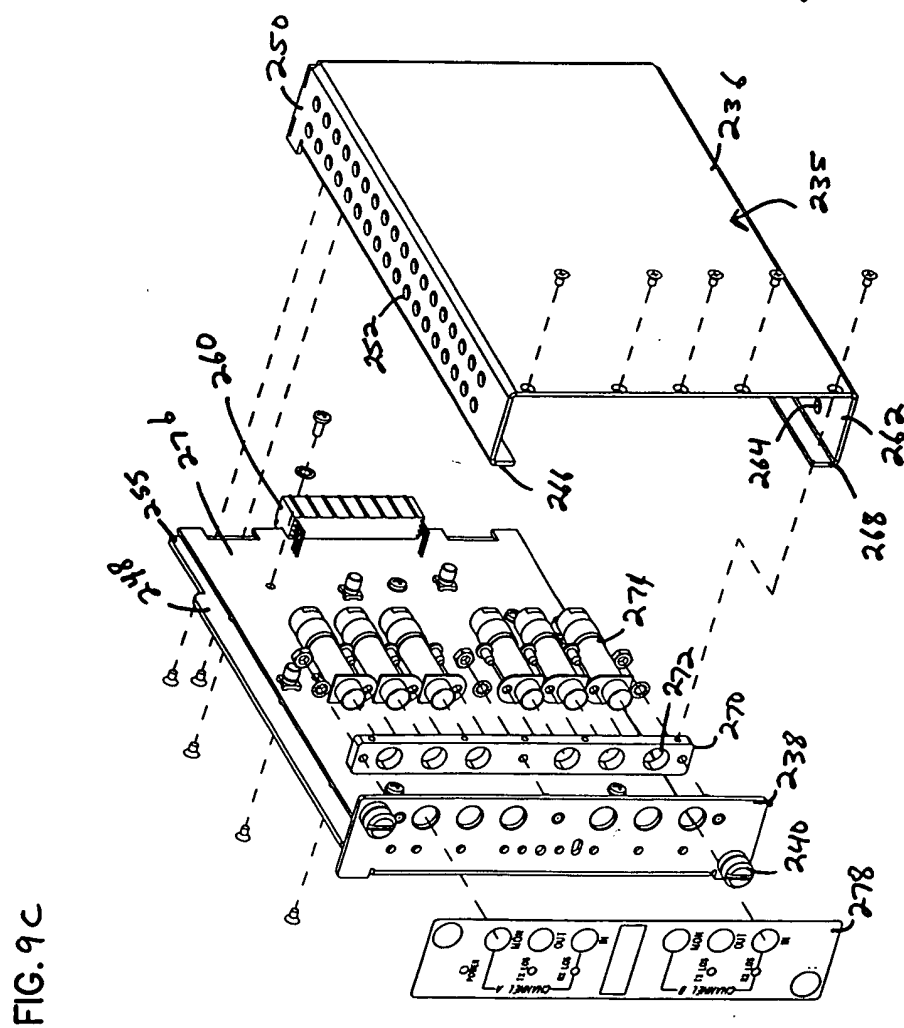
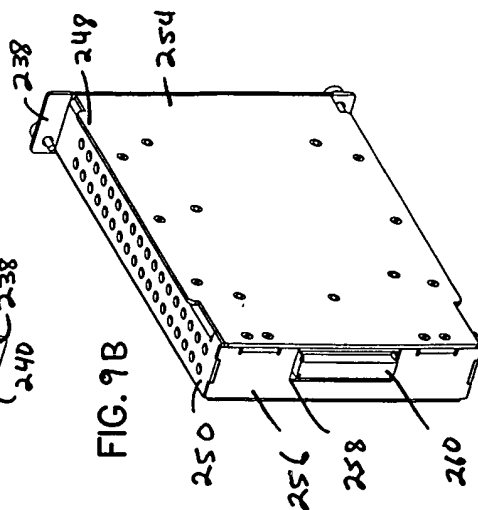
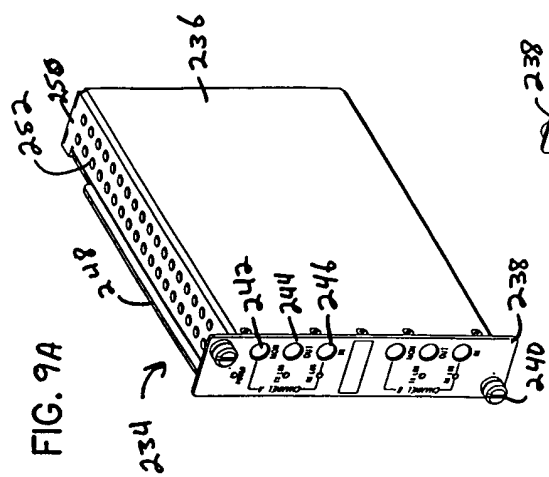


FIG. 8B



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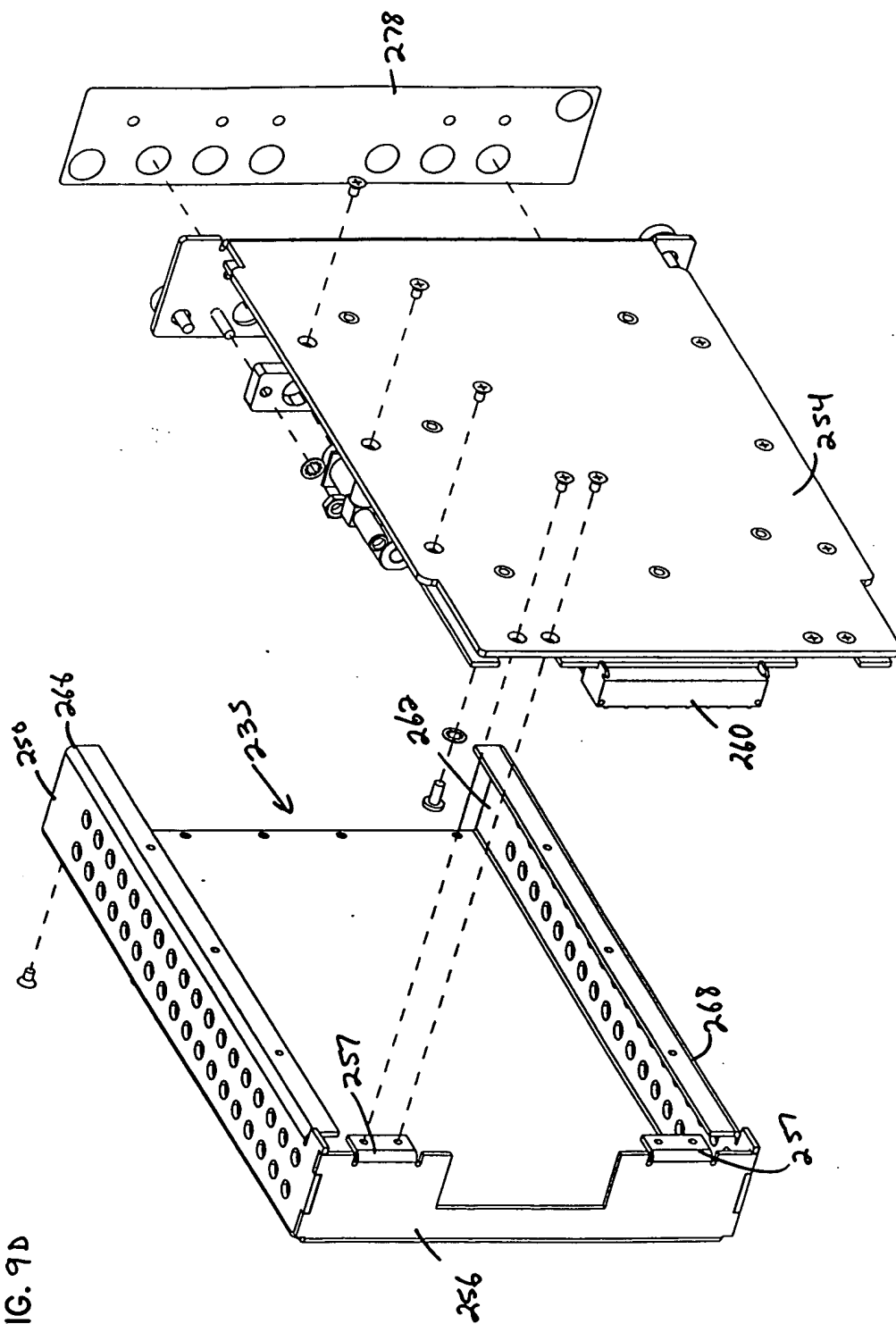


FIG. 9D

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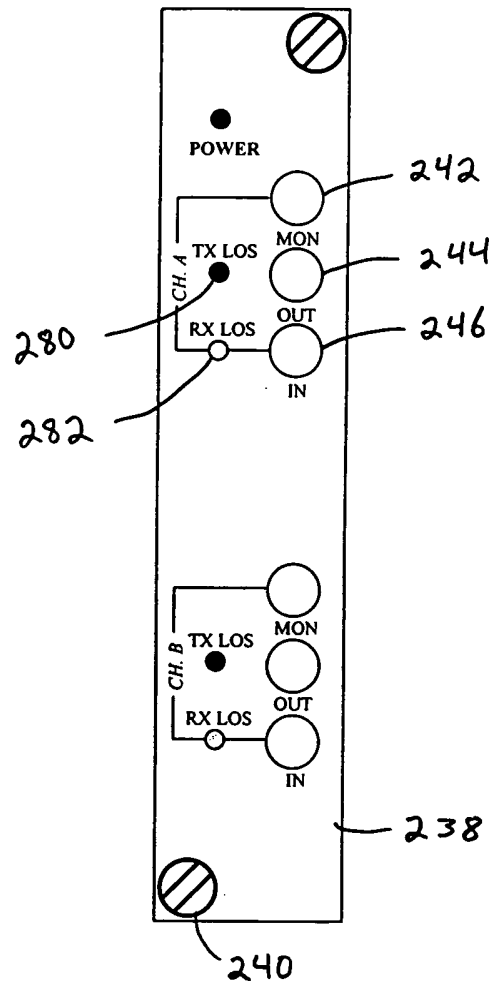


FIG. 10

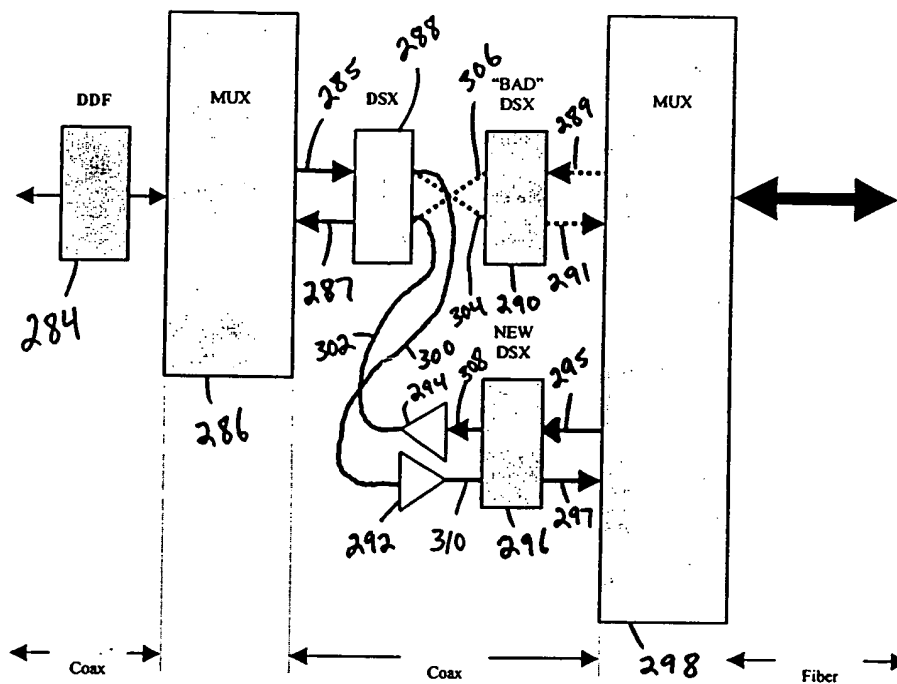


FIG. 11

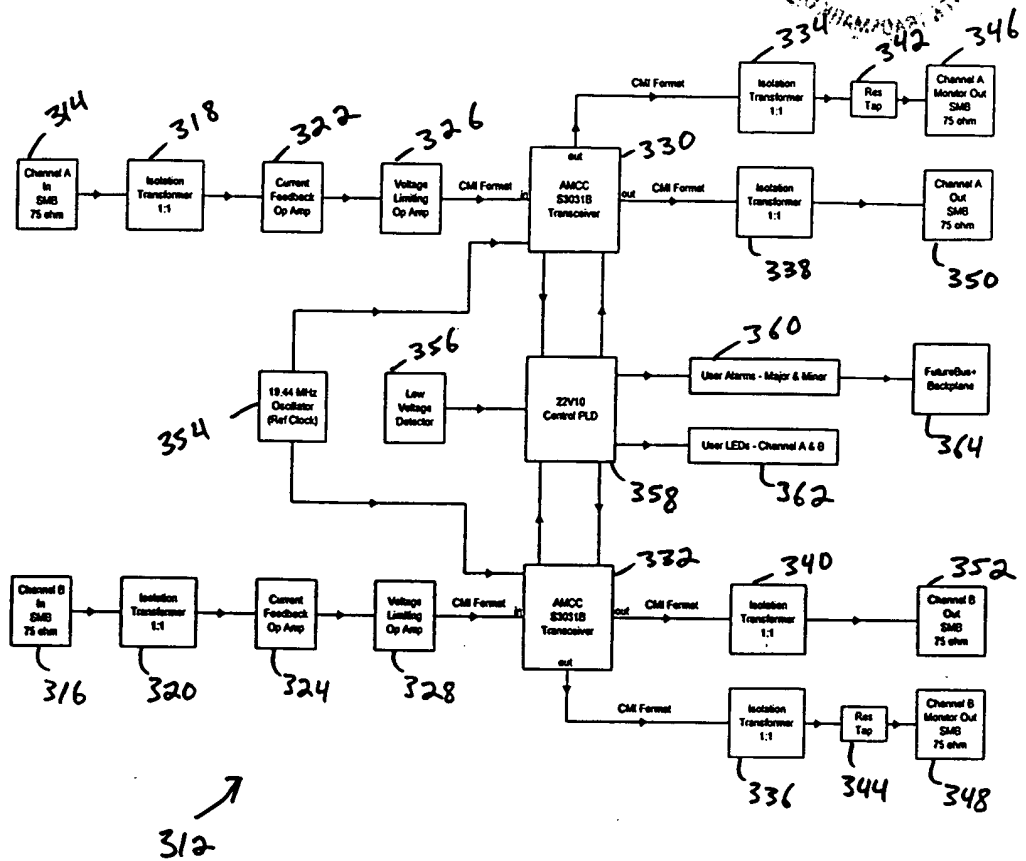
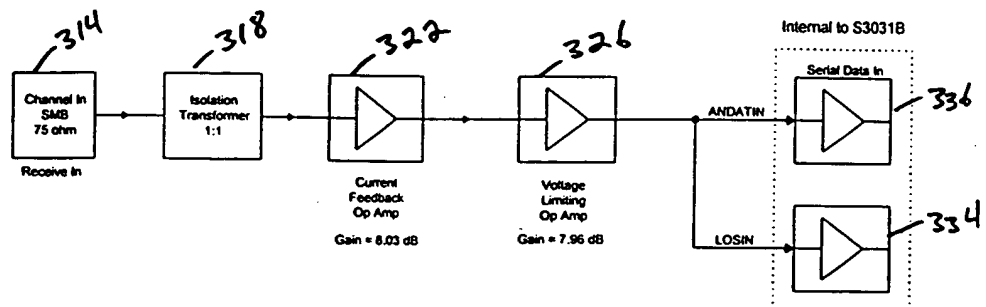


FIG. 12

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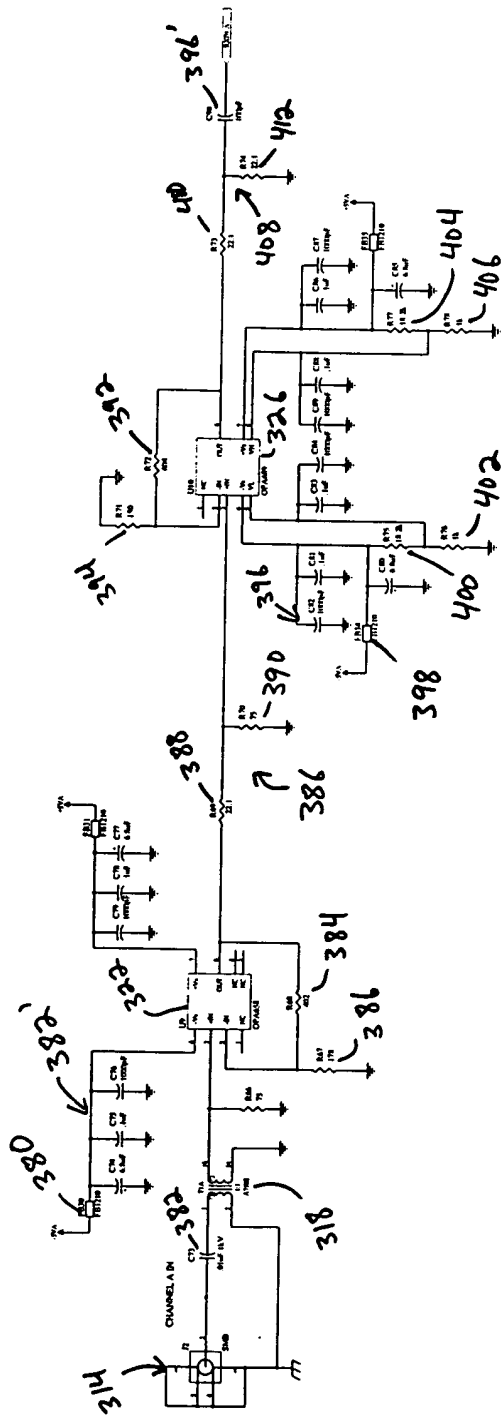


FIG. 14



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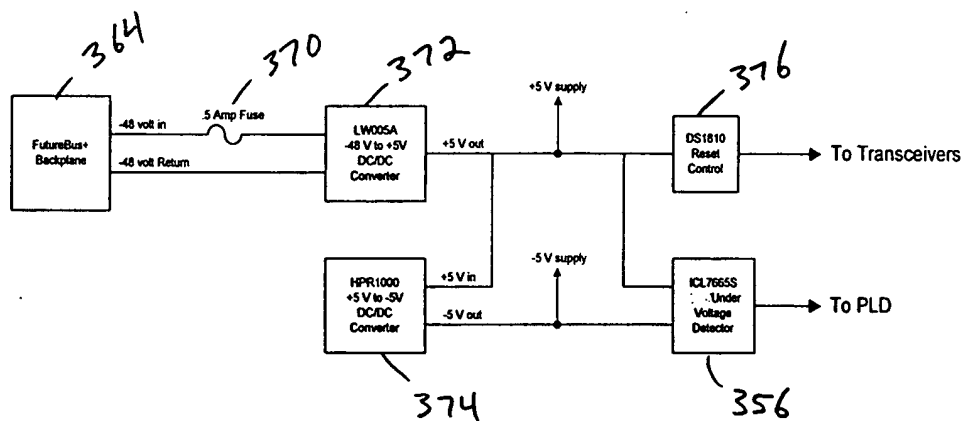
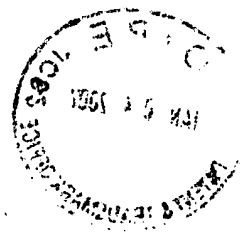
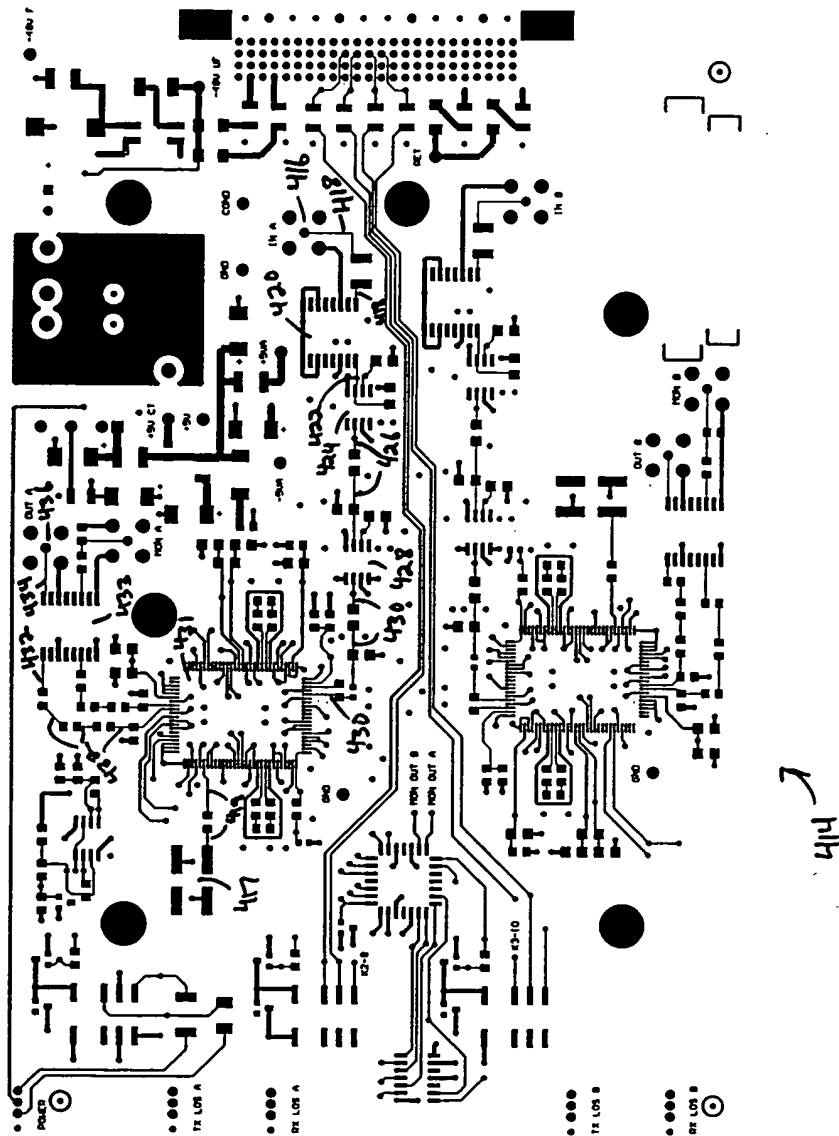


FIG. 15

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FIG. 16



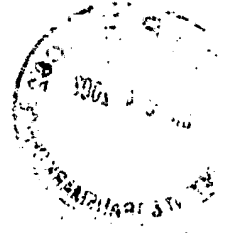
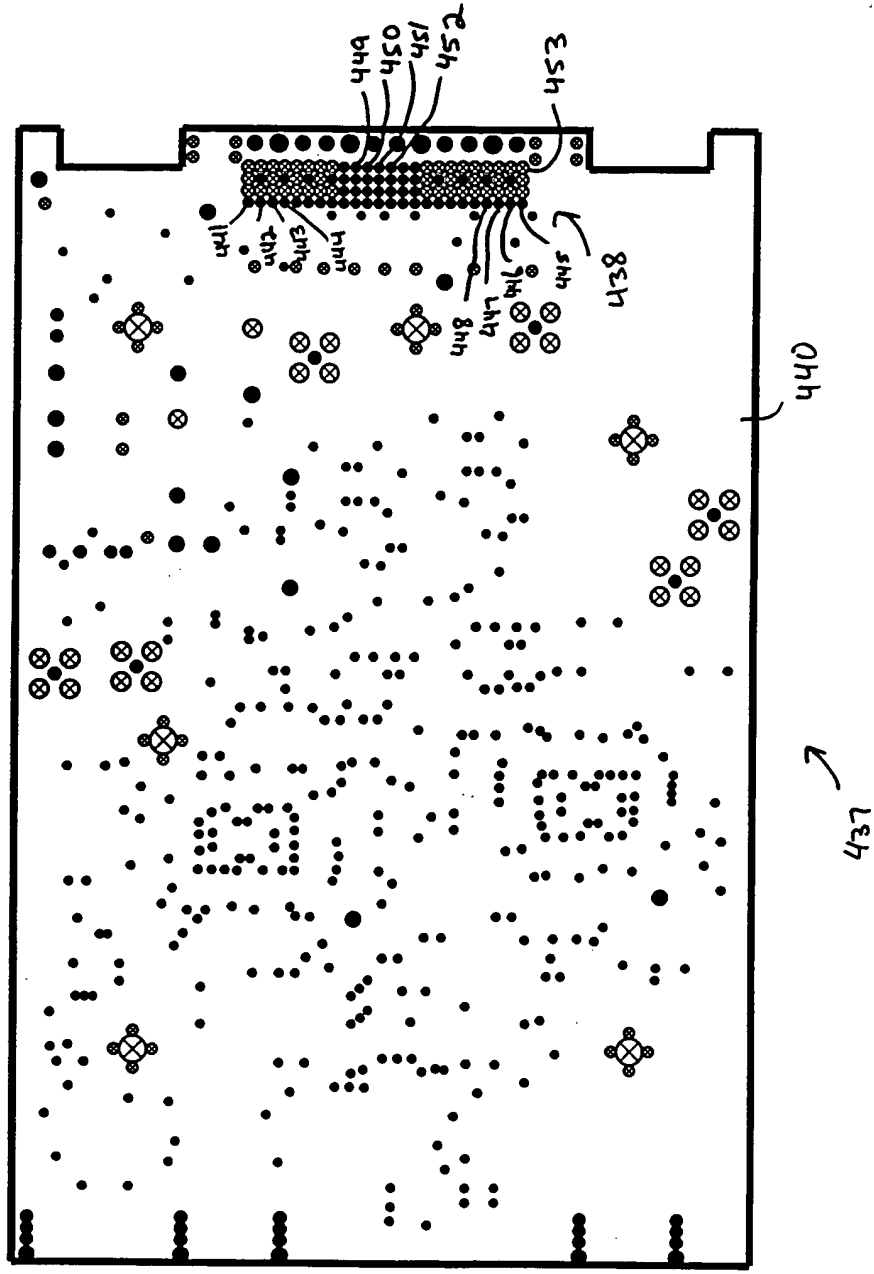


FIG. 17



6 LAYER STACK

| | |
|------------------------|-----|
| SOLDER MASK/ COMP SIDE | 462 |
| | 464 |
| | 466 |
| .008 Er = 4.3 | 468 |
| | 470 |
| .005 Er = 4.3 | 472 |
| | 474 |
| .028 Er = 4.3 | 476 |
| | 478 |
| .005 Er = 4.3 | 480 |
| | 482 |
| .008 Er = 4.3 | 484 |
| | 486 |
| SOLDER MASK/ SOD SIDE | 488 |

460 ↗

FIG. 18

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